WHAT IS CLAIMED IS:

1. A data processing method, comprising:

receiving one or more clock-data streams;

dividing said one or more clock-data streams into at least one clock stream and at least one data stream; and

synchronizing each of said at least one data stream to a common clocking domain for processing.

2. A method in accordance with claim 1, including multiplexing a plurality of said at least one data stream for processing by a framer array, said framer array being provided offset a data path of said at least one data stream.

3. A method in accordance with claim 2, further comprising aligning octets of said at least one data stream onto a multiplexed bus synchronized to said common clocking domain.

4. A method in accordance with claim 3, further comprising:

demultiplexing said plurality of at least one data stream and recombining said at least one data stream and said at least one clock stream.

5. A method according to claim 4, said at least one data stream comprising status and control information.

6. A data processing system, comprising:

means for receiving a plurality of asynchronous combined clock-data streams;

means for dividing said clock-data streams into component clock and data streams;

means for processing said data streams in a common clock domain; and

means for recombining said component clock and data streams.

7. A data processing system according to claim 6, said processing means

including a common bus onto which said component data streams are multiplexed.

8. A data processing system according to claim 7, said processing means including a framer state machine offset from said common bus adapted to align octets of said component data streams onto said common bus.

9. A data processing system according to claim 8, said processing means including a framer state machine adapted to store a context of a last data stream processed and load a context of a current data stream.

10. A system, comprising:

a plurality of clock paths adapted to extract clocks from a plurality of clock-data streams;

a plurality of data paths adapted to receive data portions of said clock-data streams and provide said data portions onto a common bus in a common clock domain; and

a framer unit offset from said common bus and adapted to load and store a context for said data portions.

11. A system according to claim 10, said framer unit further adapted to identify a start of frames of said data portions.

12. A system according to claim 11, including a plurality of synchronizers adapted to synchronize each of said plurality of data paths to said common bus.

13. A system according to claim 12, including a plurality of serial-to-parallel converters coupled to said plurality of synchronizers.

14. A system according to claim 13, wherein outputs of said serial-to-parallel converters are provided to a multiplexer.

15. A system according to claim 14, wherein outputs of said multiplexer

2 are provided to said common bus and said framer unit.

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